SONY

ICX423AL

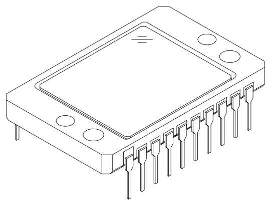
Diagonal 11mm (Type 2/3) CCD Image Sensor for CCIR B/W Video Cameras

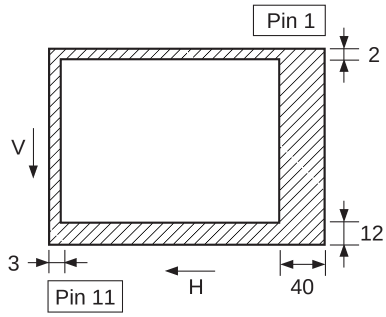
Description

The ICX423AL is an interline CCD solid-state image sensor suitable for CCIR B/W video cameras with a diagonal 11mm (Type 2/3) system. Compared with the current product ICX083AL, basic characteristics such as sensitivity and smear are improved drastically and high saturation characteristics are realized.

This chip features a field period readout system and an electronic shutter with variable charge-storage time. This chip is compatible with the pins of the ICX083AL and has the same drive conditions.

20 pin DIP (Ceramic)





Optical black position (Top View)

Features

- High sensitivity (+3.0dB compared with the ICX083AL)
- Low smear (–10.0dB compared with the ICX083AL)
- High saturation signal (+2.0dB compared with the ICX083AL)
- High resolution and Low dark current
- Excellent antiblooming characteristics
- Continuous variable-speed shutter

Device Structure

- Interline CCD image sensor
- Optical size: Diagonal 11mm (Type 2/3)
- Number of effective pixels: 752 (H) × 582 (V) approx. 440K pixels
- Total number of pixels: 795 (H) × 596 (V) approx. 470K pixels
- Chip size: 10.25mm (H) × 8.5mm (V)
- Unit cell size: 11.6µm (H) × 11.2µm (V)
- Optical black: Horizontal (H) direction: Front 3 pixels, rear 40 pixels
  Vertical (V) direction: Front 12 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 22
  Vertical 1 (even fields only)
- Substrate material: Silicon

E01X23A41

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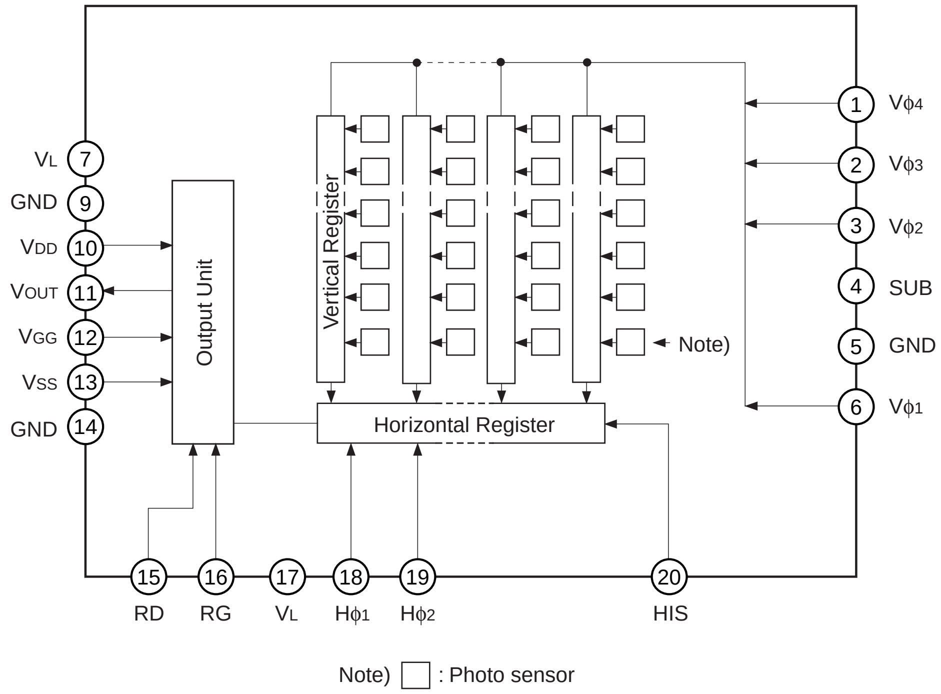
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Block Diagram and Pin Configuration

(Top view)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$V\phi 4$	Vertical register transfer clock	11	V_{OUT}	Signal output
2	$V\phi 3$	Vertical register transfer clock	12	V_{GG}	Output amplifier gate bias
3	$V\phi 2$	Vertical register transfer clock	13	V_{SS}	Output amplifier source
4	SUB	Substrate (overflow drain)	14	GND	GND
5	GND	GND	15	RD	Reset drain
6	$V\phi 1$	Vertical register transfer clock	16	RG	Reset gate clock
7	V_L	Protective transistor bias	17	V_L	Protective transistor bias
8	NC		18	$H\phi 1$	Horizontal register transfer clock
9	GND	GND	19	$H\phi 2$	Horizontal register transfer clock
10	V_{DD}	Output amplifier drain power	20	HIS	Horizontal register input source bias

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB – GND		–0.3 to +55	V	
Supply voltage	HIS, V_{DD}, RD, V_{OUT}, V_{SS} – GND	–0.3 to +20	V	
	HIS, V_{DD}, RD, V_{OUT}, V_{SS} – SUB	–55 to +10	V	
Vertical clock input voltage	Vertical clock input pins – GND	–15 to +20	V	
	Vertical clock input pins – SUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*1
Voltage difference between horizontal clock input pins		to +17	V	
$H\phi_1$, $H\phi_2$ – $V\phi_4$		–17 to +17	V	
$H\phi_1$, $H\phi_2$, RG, V_{GG} – GND		–10 to +15	V	
$H\phi_1$, $H\phi_2$, RG, V_{GG} – SUB		–55 to +10	V	
V_L – SUB		–65 to +0.3	V	
$V\phi_1$, $V\phi_3$, HIS, V_{DD}, RD, V_{OUT} – V_L		–0.3 to +30	V	
RG – V_L		–0.3 to +24	V	
$V\phi_2$, $V\phi_4$, V_{GG}, V_{SS}, $H\phi_1$, $H\phi_2$ – VL		–0.3 to +20	V	
Storage temperature		–30 to +80	°C	
Operating temperature		–10 to +60	°C	

*1 27V (Max.) when clock width < 10µs, clock duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.7	15.0	15.3	V	
Reset drain voltage	V_{RD}	14.7	15.0	15.3	V	$V_{RD} = V_{DD}$
Output amplifier gate voltage	V_{GG}	3.8	4.2	4.6	V	
Output amplifier source	V_{SS}	Ground with 750Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	9		19	V	*2
Substrate voltage adjustment precision	ΔV_{SUB}	–3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	0		3.0	V	*2
Reset gate clock voltage adjustment precision	ΔV_{RGL}	–3		+3	%	
Protective transistor bias	V_L	–11	–10.5	–10	V	*3
Horizontal register input source bias	V_{HIS}	14.7	15.0	15.3	V	$V_{HIS} = V_{DD}$

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		6		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

*2 Indications of substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) setting value
The setting value of the substrate voltage and reset gate clock voltage are indicated on the back of the image sensor by a special code. Adjust the substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the indicated voltage. The adjustment precision is ±3%.

V_{SUB} code — one character indication □ □
V_{RGL} code — one character indication ↑ ↑
V_{RGL} code V_{SUB} code

"Code" and optimal setting correspond to each other as follows.

V_{RGL} code	1	2	3	4	5	6	7
Optimal setting	0	0.5	1.0	1.5	2.0	2.5	3.0

V_{SUB} code	D	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Optimal setting	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5	19.0

<Example> "5K" → V_{RGL} = 2.0V
V_{SUB} = 12.0V

*3 This must no exceed the V_{VL} voltage of the vertical clock waveform.

*4 1) Current to each pin when 20V is applied to V_{DD}, RD, V_{OUT}, V_{SS}, HIS and SUB pins, while pins that are not tested are grounded.
2) Current to each pin when 20V is applied sequentially to $V\phi_1$, $V\phi_2$, $V\phi_3$ and $V\phi_4$ pins, while pins that are not tested are grounded. However, 20V is applied to SUB pin.
3) Current to each pin when 15V is applied sequentially to $H\phi_1$, $H\phi_2$, RG and V_{GG} pins, while pins that are not tested are grounded. However, 15V is applied to SUB pin.
4) Current to V_L pin when 30V is applied to $V\phi_1$, $V\phi_3$, HIS, V_{DD}, RD and V_{OUT} pins or when, 24V is applied to RG pin or when, 20V is applied to $V\phi_2$, $V\phi_4$, V_{GG}, V_{SS}, $H\phi_1$ and $H\phi_2$ pins, while V_L pin is grounded. However, GND and SUB pins are left open.

*5 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

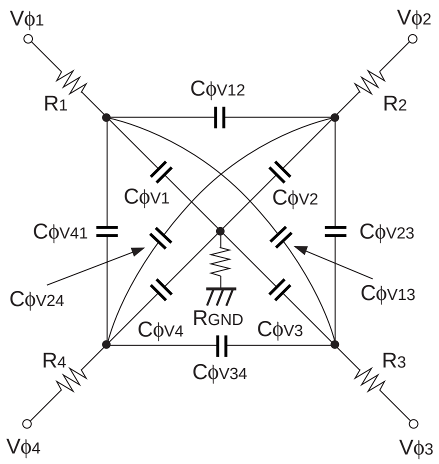
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.5	15.0	15.5	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}, V_{VH3}, V_{VH4}	–0.6		0	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}		–9.6		V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V_{\phi V}$	8.9			V	2	$V_{\phi V} = V_{VH}n - V_{VL}n$ (n = 1 to 4)
	$\| V_{VH1} - V_{VH2} \|$			0.2	V	2	
	$V_{VH3} - V_{VH}$	–0.5		0	V	2	
	$V_{VH4} - V_{VH}$	–0.5		0	V	2	
	V_{VHH}			0.8	V	2	High-level coupling
	V_{VHL}			1.0	V	2	High-level coupling
	V_{VLH}			0.8	V	2	Low-level coupling
	V_{VLL}			0.8	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	6.0		8.0	V	3	
	V_{HL}	–3.5		–3.0	V	3	
Reset gata clock voltage	$V_{\phi RG}$	6.0		13.0	V	3	*1
	V_{RGL}	0		3.0	V	3	
Substrate clock voltage	$V_{\phi SUB}$	27.0		32.0	V	4	

*1 The reset gate clock voltage need not be adjusted when the reset gate clock is driven when the specifications are as given below. In this case, the reset gate clock voltage setting indicated on the back of the image sensor has not significance.

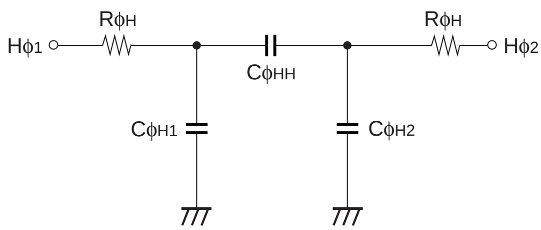
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	–0.2	0	0.2	V	3	
	$V_{\phi RG}$	8.5	9.0	9.5	V	3	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		2700		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		2700		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		2600		pF	
	$C_{\phi V23}$, $C_{\phi V41}$		950		pF	
	$C_{\phi V13}$		1000		pF	
	$C_{\phi V24}$		500		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		47		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		58		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		7		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		800		pF	
Vertical transfer clock series resistor	R_1, R_2, R_3, R_4		22		Ω	
Vertical transfer clock ground resistor	R_{GND}		3		Ω	
Horizontal transfer clock series resistor	$R_{\phi H}$		10		Ω	



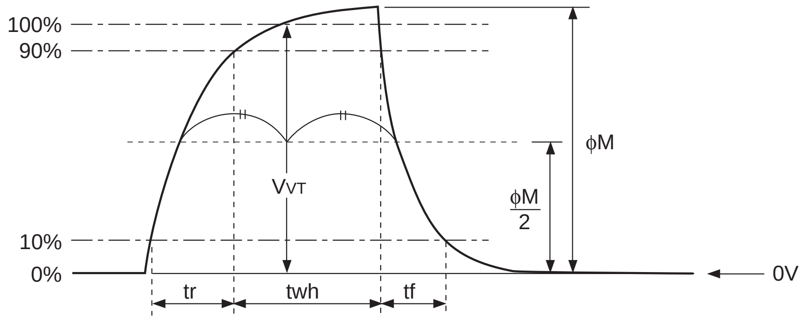
Vertical transfer clock equivalent circuit



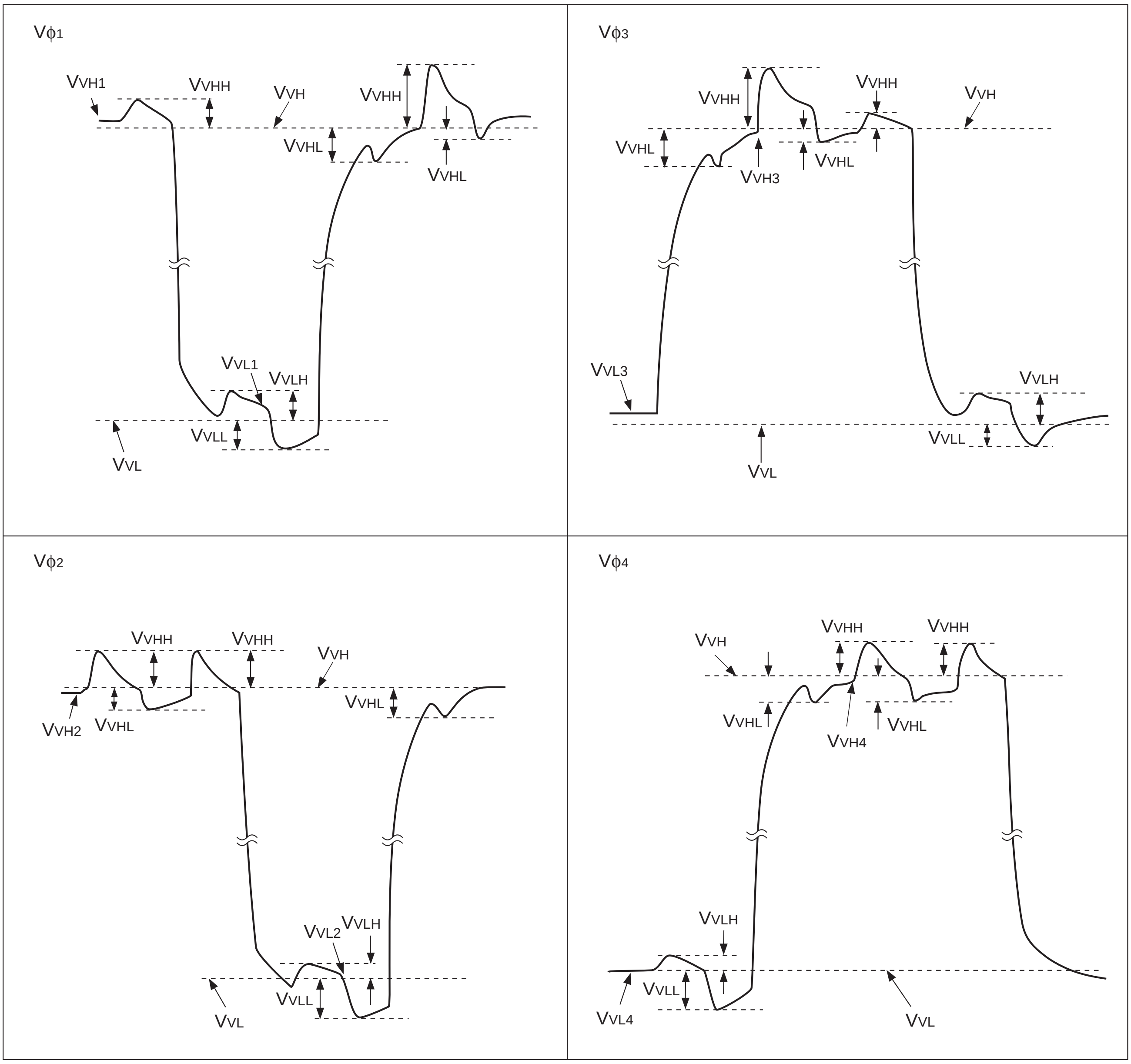
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform

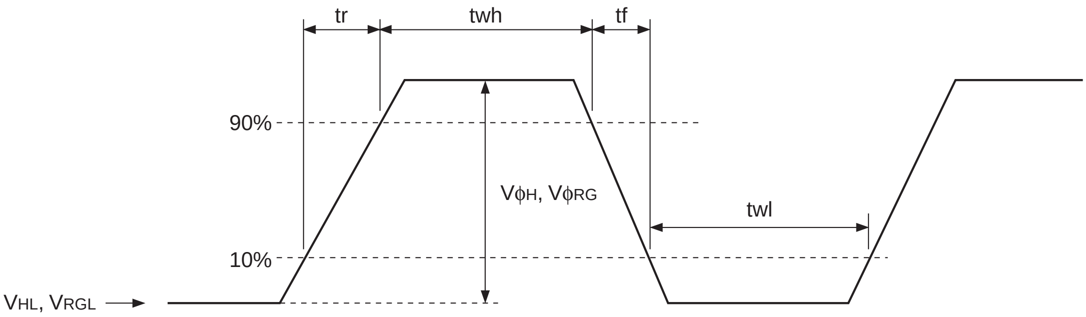


(2) Vertical transfer clock waveform

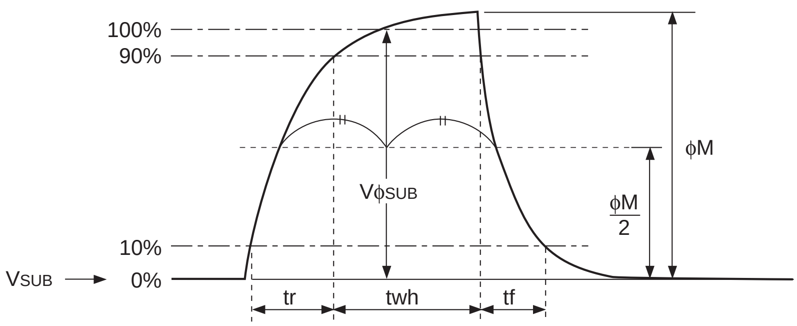


$V_{VH} = (V_{VH1} + V_{VH2})/2$
$V_{VL} = (V_{VL3} + V_{VL4})/2$
$V_{\phi V} = V_{VH}n - V_{VL}n$ (n = 1 to 4)

(3) Horizontal transfer clock waveform · Reset gate clock waveform



(4) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.3	2.5						0.5			0.5		µs	During readout
Vertical transfer clock	$V\phi_1$, $V\phi_2$		62.6			0.74			0.1			0.1		µs	During imaging
	$V\phi_3$, $V\phi_4$		1.3			62.1			0.1			0.1		µs	
Horizontal transfer clock	Hφ		20			20			15	19		15	19	ns	During imaging
	$H\phi_1$		5.38						0.01			0.01		µs	During parallel-serial conversion
	$H\phi_2$					5.38			0.01			0.01		µs	
Reset gate clock	φRG	11	13			51			2.0			2.0		ns	
Substrate clock	φSUB	1.5	1.8							0.5			0.5	µs	When draining charge

Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	700	1000		mV	1	
Saturation signal	Vsat	1000			mV	2	Ta = 60°C
Smear	Sm		–130	–120	dB	3	
Video signal shading	SH			25	%	4	
Dark signal	Vdt			2	mV	5	Ta = 60°C
Dark signal shading	ΔVdt			1	mV	6	Ta = 60°C
Flicker	F			5	%	7	
Lag	Lag			0.5	%	8	

Image Sensor Characteristics Measurement Method

◎**Measurement conditions**

1) In the following measurements, the substrate voltage and the reset gate clock voltage are set to the values indicated on the device, and the device drive conditions are at the typical values of the bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, and the value measured at point [*A] in the drive circuit example is used.

◎**Definition of standard imaging conditions**

1) Standard imaging condition I:
Use a pattern box (luminance 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.00mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity luminous intensity.

2) Standard imaging condition II :
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.00mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output (Vs) at the center of the screen and substitute the value into the following formula.

$$S = Vs \times \frac{250}{50} \quad [mV]$$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with average value of signal output, 350mV, measure the minimum value of the signal output.

3. Smear
   Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with average value of the signal output, 350mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (VSm [mV]) of the signal output and substitute the value into the following formula.

   $$Sm = 20 \times \log \left(\frac{VSm}{350} \times \frac{1}{500} \times \frac{1}{10} \times 100 \right) \text{ [dB] (1/10V method conversion value)}$$

4. Video signal shading
   Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 350mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

   $SH = (Vmax - Vmin)/350 \times 100$ [%]

5. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

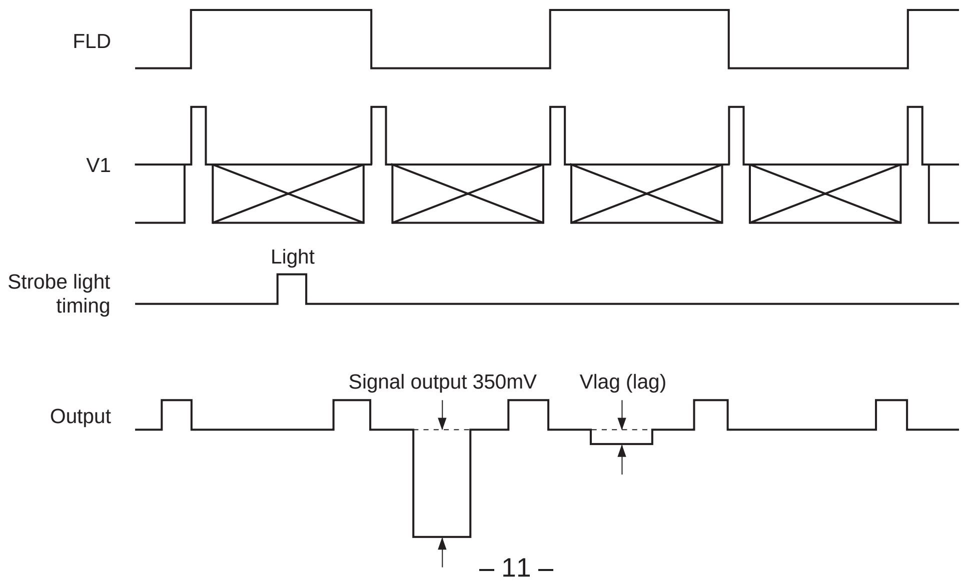
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

7. Flicker
   Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the signal output is 350mV, and then measure the difference in the signal level between fields (ΔVf [mV]). Then substitute the value into the following formula.

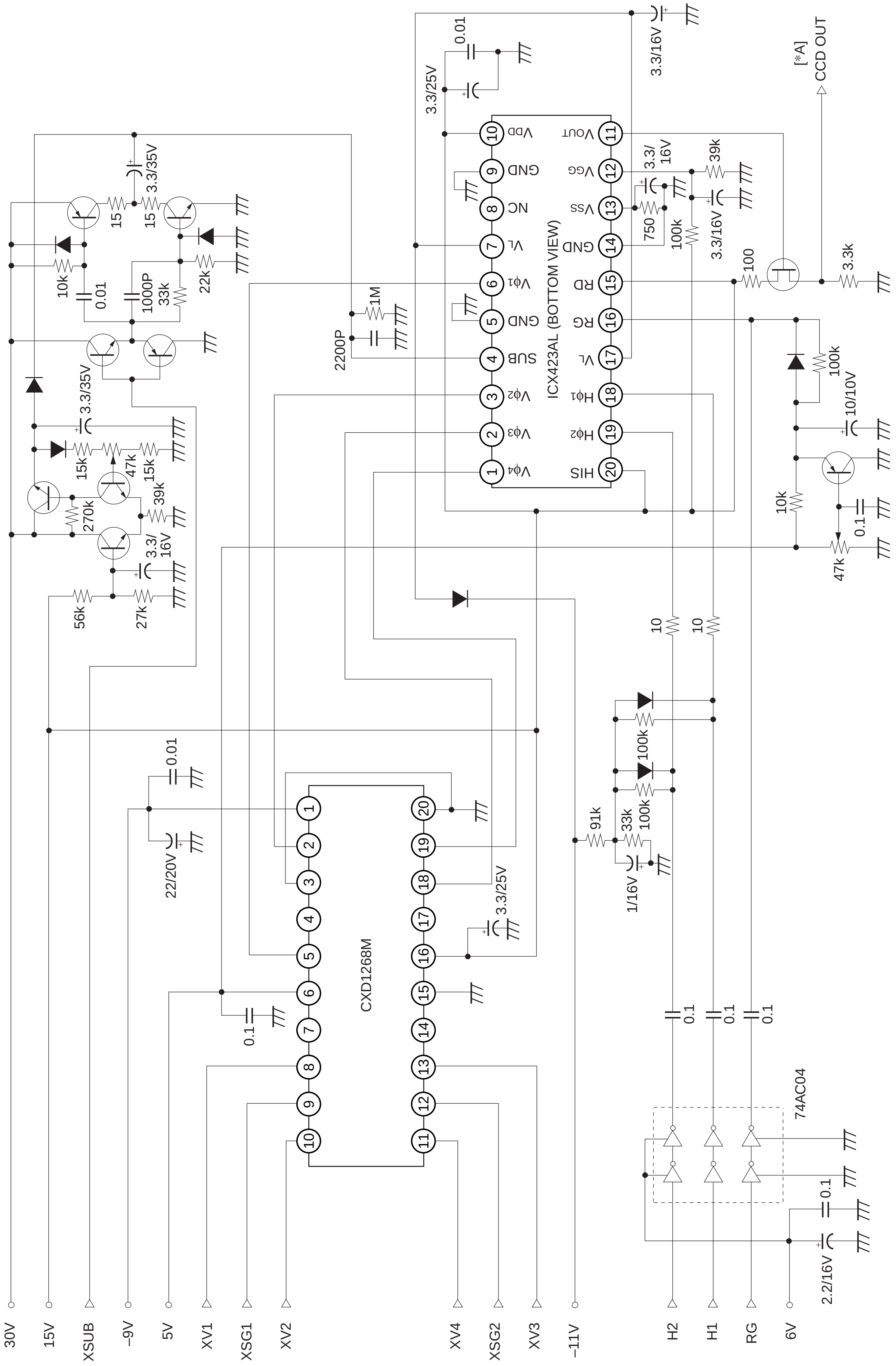
   $F = (\Delta Vf/350) \times 100$ [%]

8. Lag
   Adjust the signal output value generated by strobe light to 350mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

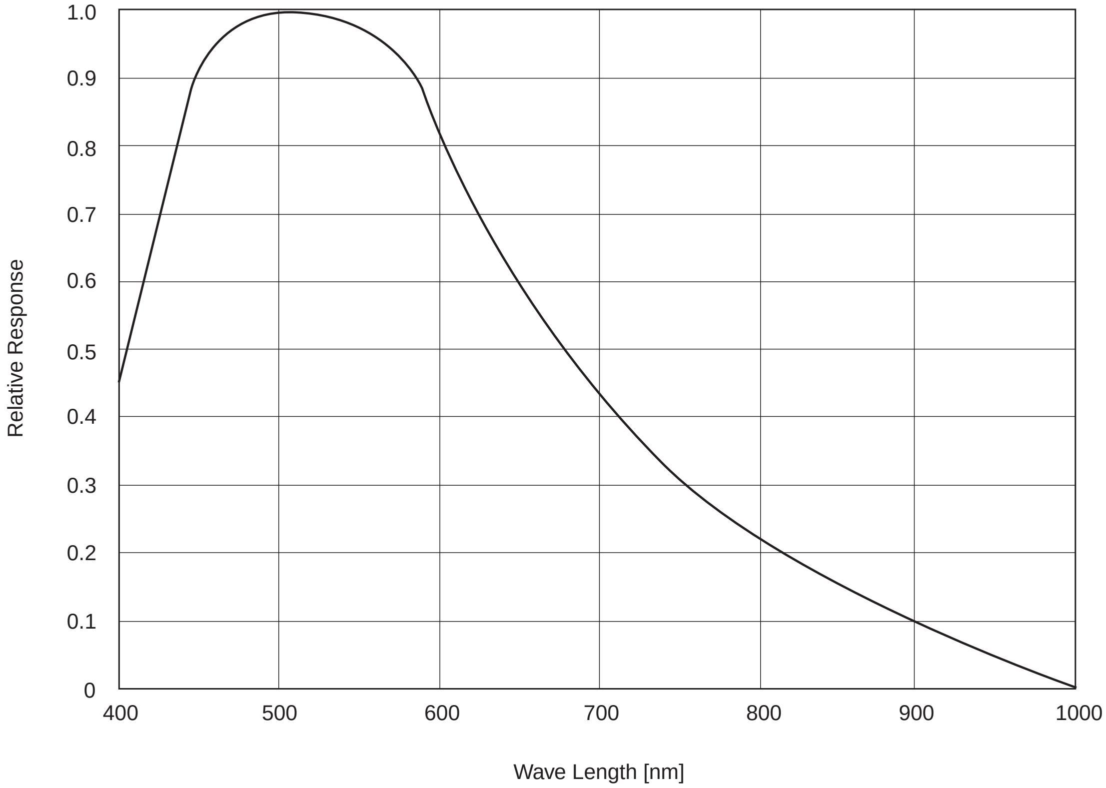
   $Lag = (Vlag/350) \times 100$ [%]



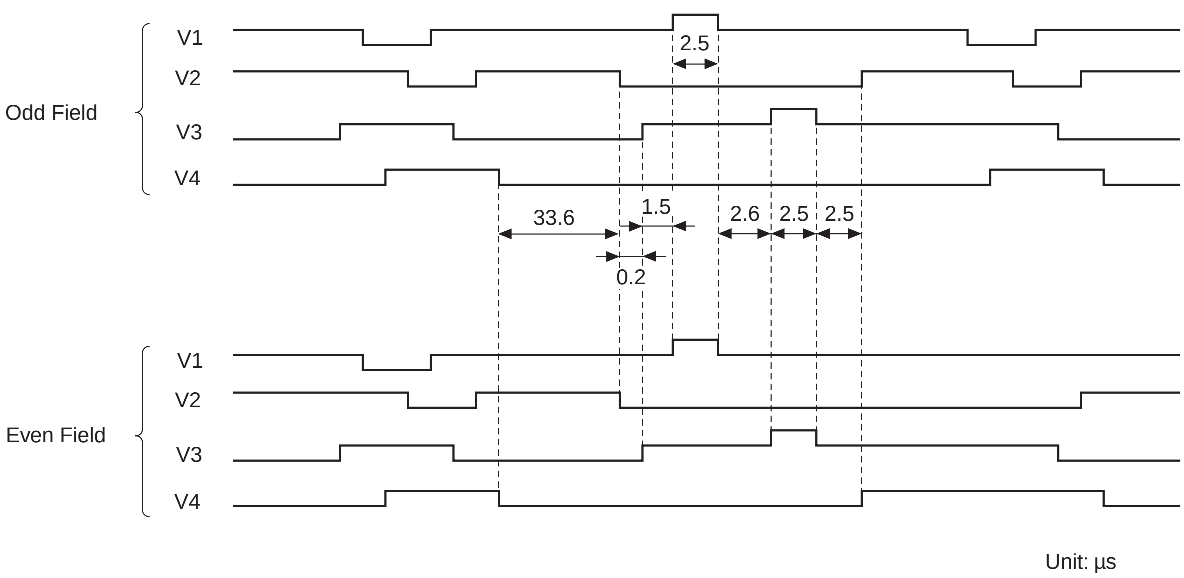
Drive Circuit



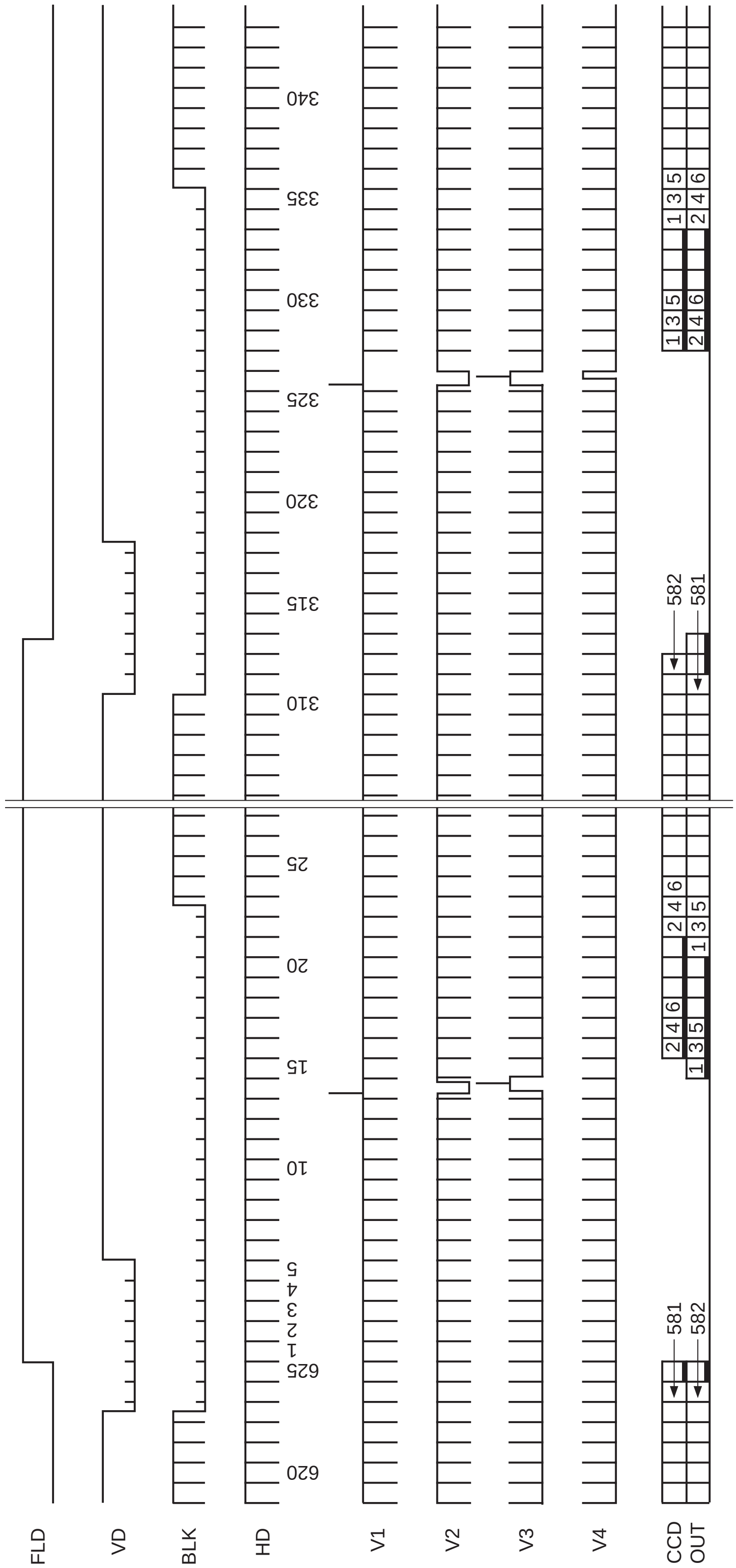
Spectral Sensitivity Characteristics (includes lens characteristics, excludes light source characteristics)



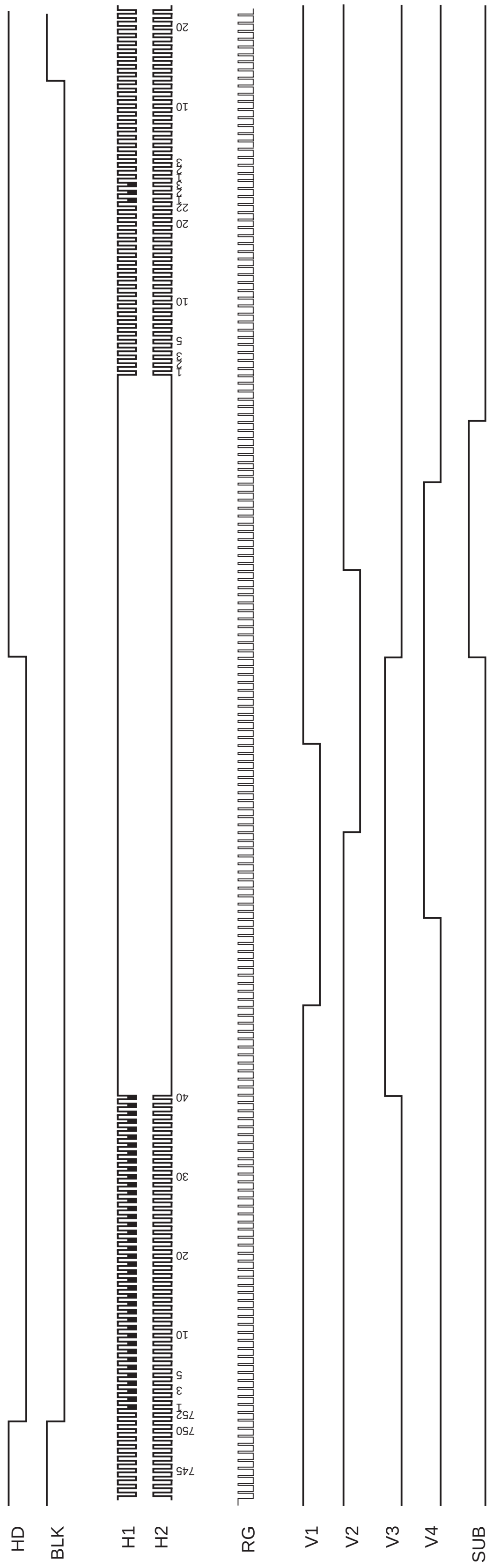
Sensor Readout Clock Timing Chart



Drive Timing Chart (Vertical Sync)



Drive Timing Chart (Horizontal Sync)



Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.
   a) Operate in clean environments (around class 1000 is appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

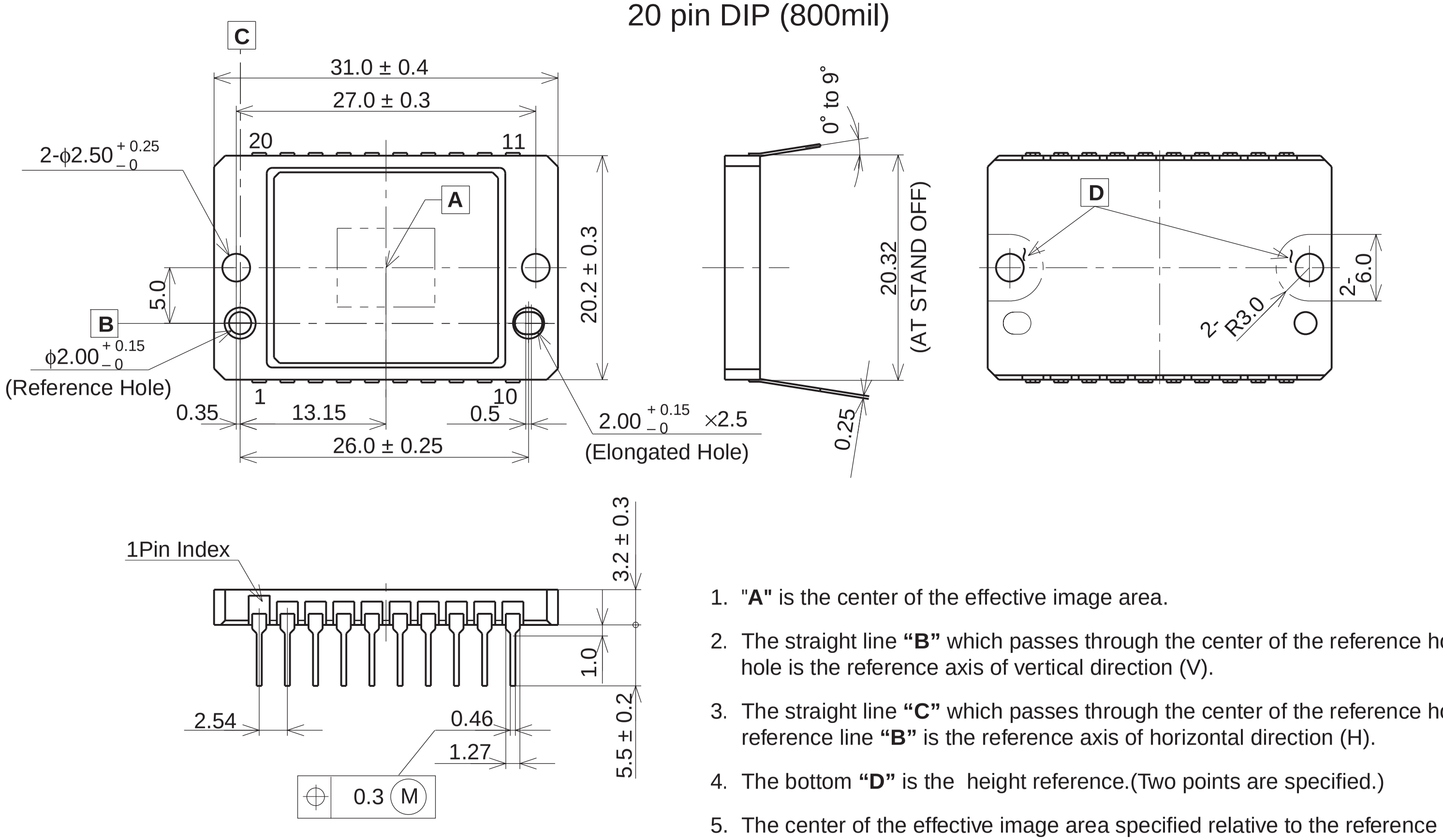
4) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

Package Outline Unit: mm

20 pin DIP (800mil)



PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.90g
DRAWING NUMBER	AS-A11(E)

1. "**A**" is the center of the effective image area.
2. The straight line **"B"** which passes through the center of the reference hole and the elongated hole is the reference axis of vertical direction (V).
3. The straight line **"C"** which passes through the center of the reference hole at right angle to vertical reference line **"B"** is the reference axis of horizontal direction (H).
4. The bottom **"D"** is the height reference.(Two points are specified.)
5. The center of the effective image area specified relative to the reference hole is (H, V) = (13.15, 5.0) ± 0.15mm.
6. The angle of rotation relative to the reference line **"B"** is less than ± 1°
7. The height from the bottom **"D"** to the effective image area is 1.46 ± 0.15mm.
8. The tilt of the effective image area relative to the bottom **"D"** is less than 60µm.
9. The thickness of the cover glass is 0.75mm and the refractive index is 1.5.